a scan-path interface circuit for reading out contents of a predetermined memory or register in said system;

a switching circuit coupled to said processor and to said scan-path interface circuit for switching said scan-path interface circuit between a first mode in which it is enabled and a second mode in which it is disabled; and

security means comprising:

a plurality of input ports for said processor;

a program stored in said memory to operate said process to receive a plurality of commands applied to said plurality of input ports and to process said commands to produce a password which is compared with a predetermined password;

and wherein said switching circuit is responsive to said comparison.

5. (new) The computer system of claim 4 wherein said program operates said processor to receive said plurality of commands which are applied to said plurality of ports in a specific time sequence.

6. (new) The computer system of claim 4 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

7. (new) The computer system of claim 5 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

8. ( new) In an integrated circuit computer system having a processor interconnected with memory and peripheral circuits on said integrated circuit and coupled to a scan-path interface circuit, a security system comprising:

a plurality of input ports for said processor;

a program stored in said memory to operate said processor to received a plurality of commands applied to said plurality of input ports and to process said commands to produce a password which is compared with a predetermined password.

9. (new) The security system of claim 8 further comprising a switching circuit coupled to said scan-path interface circuit and responsive to said comparison for switching said scan-path interface circuit between a first mode in which it is enabled and a second mode in which it is disabled.

10. (new) The security system of claim 8 wherein said program operates said processor to receive said plurality of commands which are applied to said plurality of ports in a specific time sequence.

11. (new) The security system of claim 8 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

12. (new) The security system of claim 9 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

13. (new) The security system of claim 10 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

14. (new) A security system for an integrated circuit computer system comprising:

means for applying a plurality of commands to a plurality of ports for a processor of said system;

a program stored in a memory coupled to said processor for operating said processor to process said plurality of commands to produce a password;

means for comparing said produced password with a predetermined password.

15. (new) The security system of claim 14 wherein said program operates said processor to receive said plurality of commands which are applied to said plurality of ports in a specific time sequence.

16. (new) The security system of claim 14 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers and generating a comparison signal.

17. (new) The security system of claim 15 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers and generating a comparison signal.

18. (new) The security system of claim 14 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and disabled modes.

19. (new) The security system of claim 15 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and a disable modes.

20. (new) The security system of claim 16 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit

responsive to said comparison to switch operation of said scan-path interface circuit between enabled and a disable modes.

21. (new) The security system of ~~claim 17 further~~ comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said ~~system and a~~ switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and a disable modes.--

In the Drawings:

A proposed drawing correction is enclosed herewith.